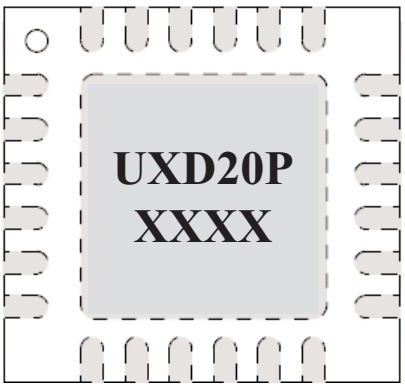
DC - 20 GHz Programmable 1,2,4,8 Binary Prescaler

Features

- Wide Operating Range: DC - 20GHz
- Low SSB Phase Noise: -153 dBc @ 10kHz
- Large Output Swings: 750mV ppk/side
- Single-Ended and/or Differential Operation
- Low Power Consumption: 430mW
- 4x4 QFN Package
- 3 Dividers-in-One with Pass Through
- DC-7 GHz Limit Amp



24 pin Quad Flat No Lead (QFN)
4x4 mm pkg, 0.5mm pad pitch
JEDEC MO-220 Compliant

Marking Information:
UXD20P = Device Part Number
XXXX = Lot Code

Description

The UXD20P is a low noise DC to 20GHz programmable prescaler featuring either divide by-1, divide-by-2, divide-by-4, or divide-by-8 division ratios. In the divide by 1 mode the UXD20P is also a DC-7 GHz limit amplifier. The device features differential inputs and outputs, adjustable output swing and high input sensitivity. The control inputs are CMOS and LVTTL compatible. The UXD20P is packaged in a 24 pin, 4mm x 4mm leadless surface mount package.

Pad Metallization

The QFN package pad metallization consists of a 300-800 micro-inch (typical thickness 435 micro-inch or 11.04um) 100% matte Sn plate. The plating covers a Cu (C194) leadframe. The packages are manufactured with a >1hr 150C annealing/heat treating process, and the matte (non-glossy) plating, specifically to mitigate tin whisker growth.

Application

The UXD20P can be used as a general purpose, fixed modulus prescaler in high frequency PLLs. The low phase noise of the divider makes it ideal for generating low jitter, synchronous clocks in telecom applications.

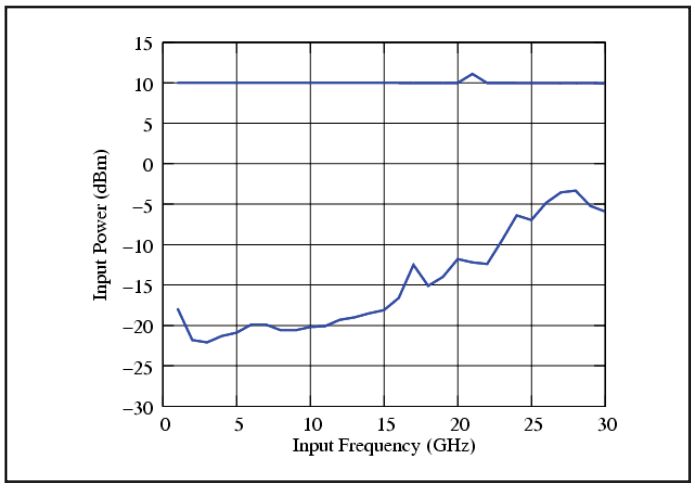
Key Specifications (T=25 ºC)

Vee = -3.3V, Iee = 130mA, Zo = 50Ω

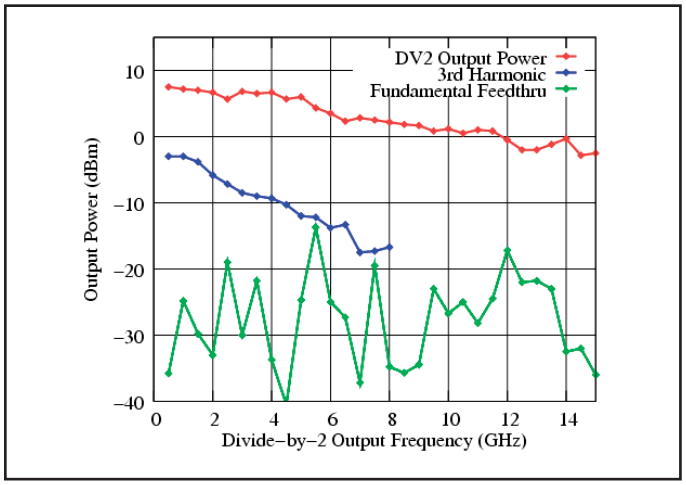
Parameter	Description	Minimum	Typical	Maximum
F_{in} (GHz)	Input Frequency	DC*	-	20
P_{in} (dBm)	Nominal Input Power	-10	0	+10
P_{out} (dBm)	Nominal Output Power	-5	+5	-
£(dBc/Hz)	SSB Phase Noise @10kHz Offset	-	-153	-
Pdc (mW)	DC Power Dissipation	-	430	-
$P_{spitback}$ (dBm)	Freq/2 Power Spitback @Input	-	TBD	-
$P_{fundamental}$ (dBm)	Fundamental Feedthru @Output	-	TBD	-

*Low frequency limit dependent on input edge speed

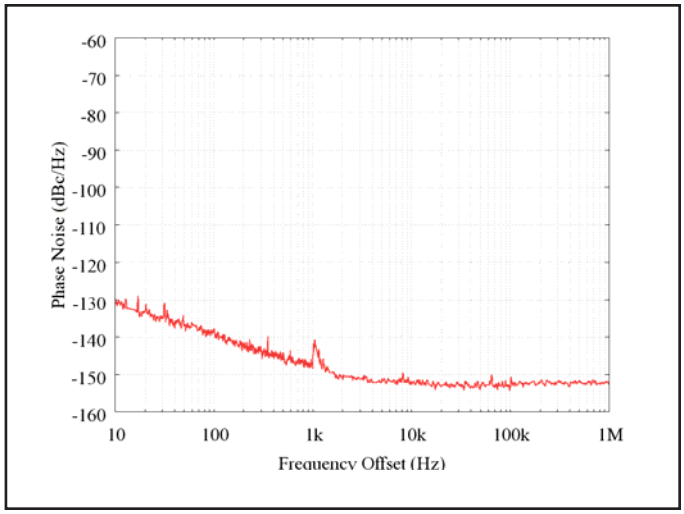
Frequency Divider Application



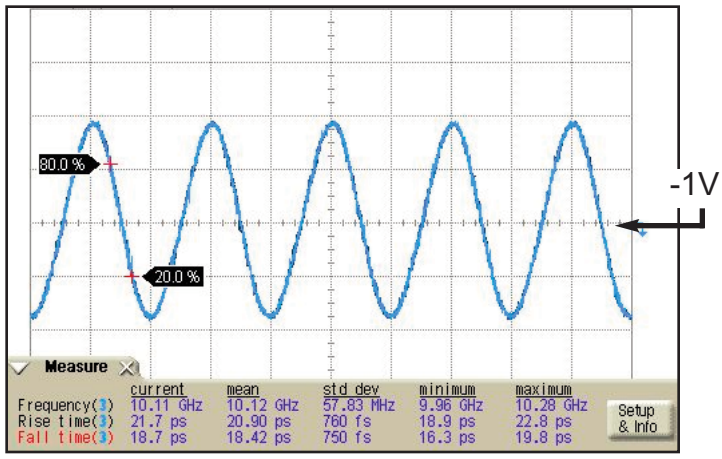
Min/Max Single-Ended Power
Input Sensitivity Window



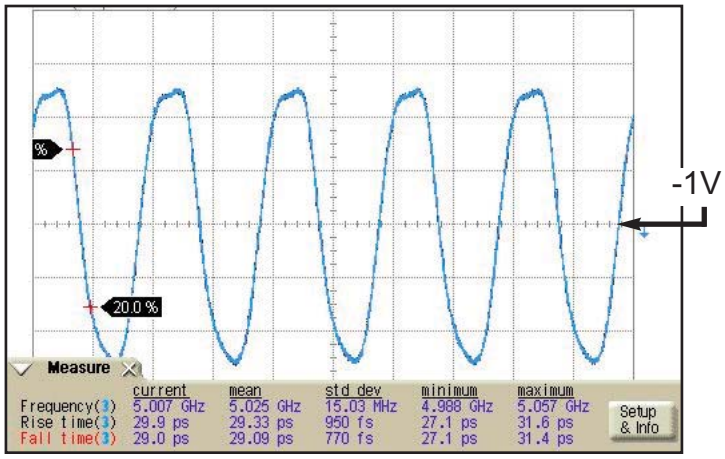
Binary Divide-by-2 Output Power,
3rd Harmonic & Input Feedthru



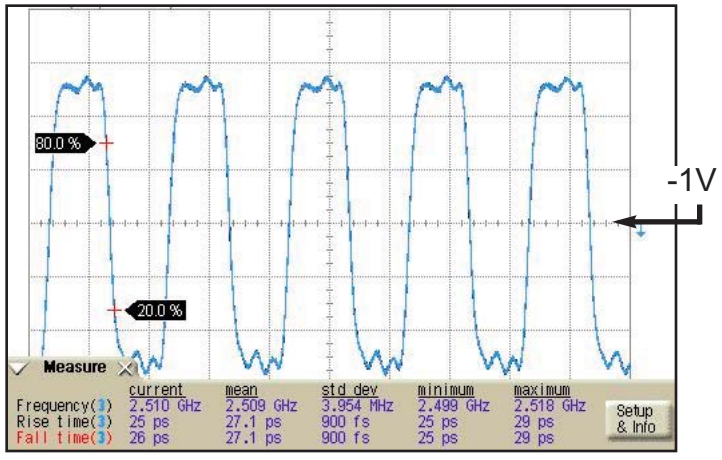
UXD20P: SSB Phase Noise for Binary Divide-by-8
Configuration Input Freq = 7.8 GHz
Gain S21



Binary Divide-by-2 Configuration
Input Freq = 20 GHz, 150mV/div

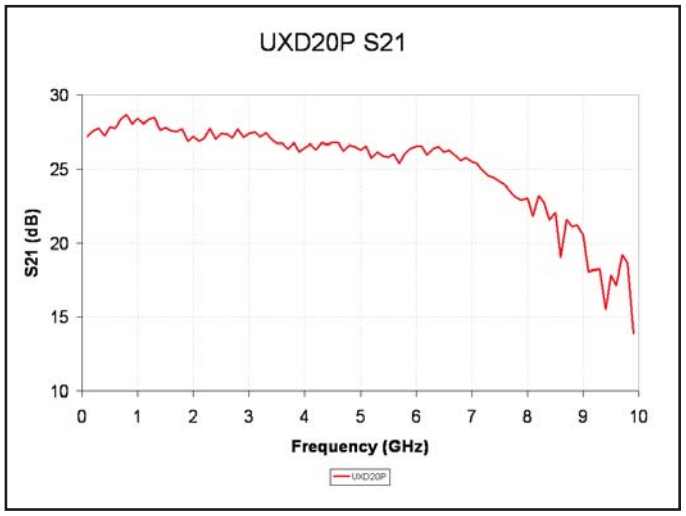


Binary Divide-by-4 Configuration
Input Freq = 20 GHz, 150mV/div

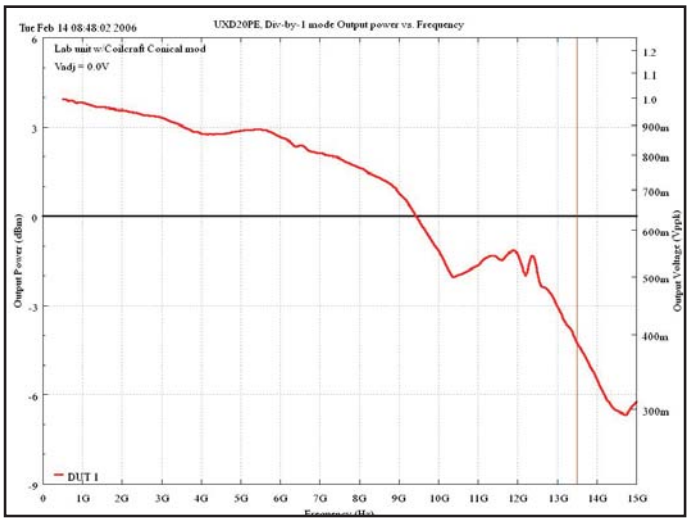


Binary Divide-by-8 Configuration
Input Freq = 20 GHz, 150mV/div

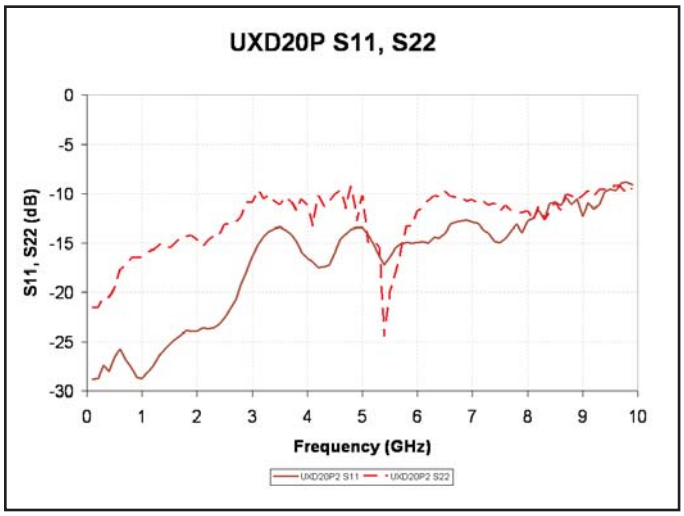
Limit Amplifier Application



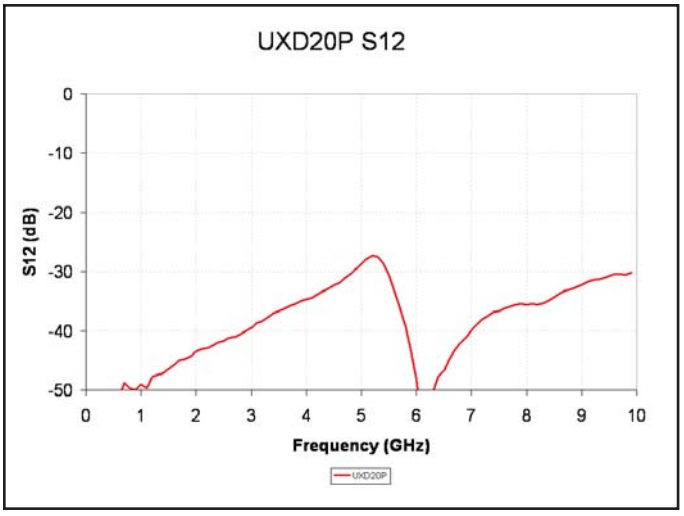
S-parameters S21



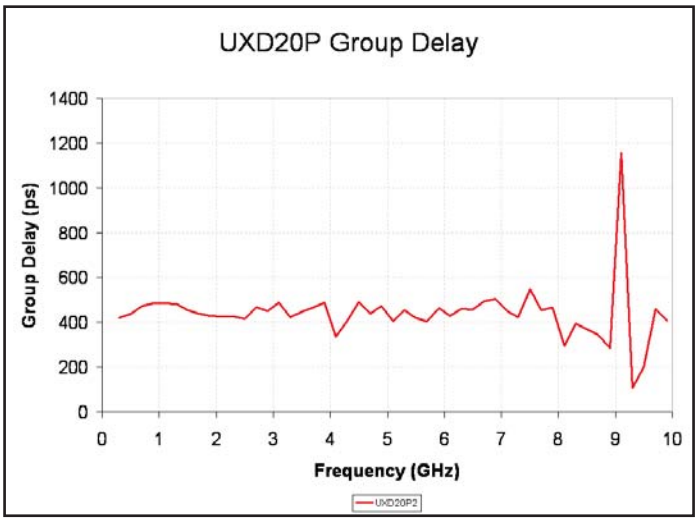
Pout vs. Frequency



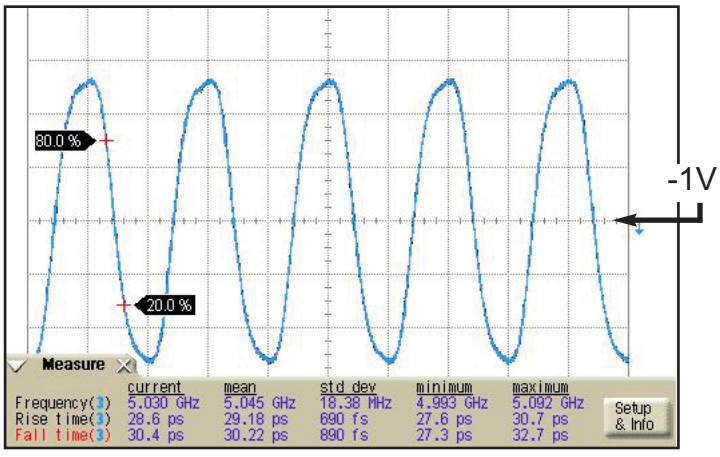
S-parameters S11, S22



S-parameters S12

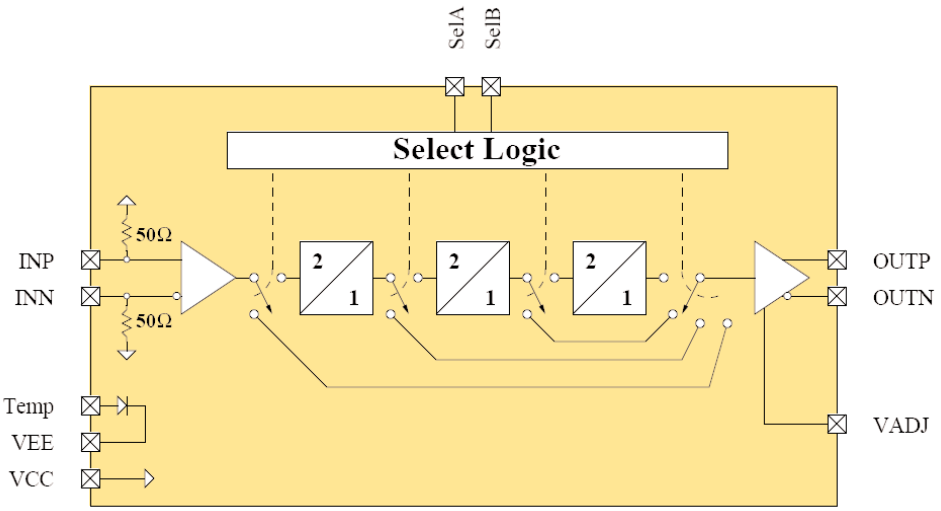


Group Delay vs. Frequency



Binary Divide-by-1 Configuration
Input Freq = 5 GHz, 150mV/div

Functional Block Diagram



Pin Description

Port Name	Description	Additional Comments
INP	Prescaler Input, Positive Terminal	Negative CML signal levels
INN	Prescaler Input, Negative Terminal	Negative CML signal levels
OUTP	Prescaler Output, Positive Terminal	Requires DC return path to VCC
OUTN	Prescaler Output, Negative Terminal	Requires DC return path to VCC
VADJ	Output Amplitude Control	Tie to VCC via resistor, refer to text for value
SelA	Divider Select Control Line	Divider Select, See Table 1, defaults to logic 0
SelB	Divider Select Control Line	Divider Select, See Table 1, defaults to logic 0
Temp	Temperature Diode	Optional Temperature diode, refer to text
VCC	RF & DC Ground	-
VEE	-3.3V @ 130mA	Negative Supply Voltage

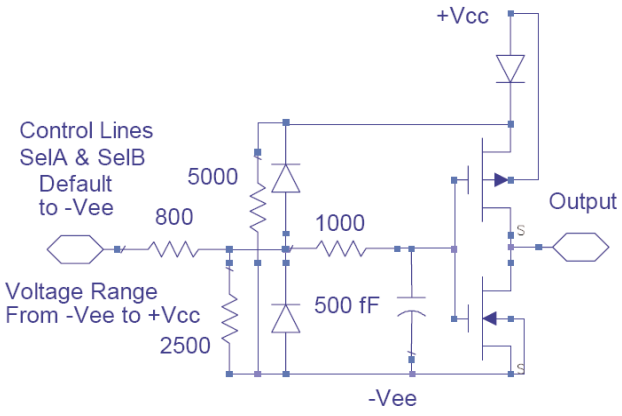
Table 1: Divider Mode Select Logic

SelA	SelB	Mode	DC Current
0	0	Divide-by-1	105 mA
1	0	Divide-by-8	130 mA
0	1	Divide-by-4	125 mA
1	1	Divide-by-2	120 mA

Table 2: Control Voltages

State	Bias Condition	Comment
Low (logic 0)	VEE @ 0 mA	Default condition (internally pulled low)
High (logic 1)	VCC @ 1 mA	

Simplified Control Logic Schematic



Application Notes

Divider Mode

The UXD20P supports four division ratios controlled by two select lines which are compatible with CMOS/LVTTL signaling levels. Table 1 lists the four states for the given logic levels on the SelA and SelB select lines. For any of the four modes, circuitry which is not used is automatically powered down to reduce power consumption.

Divider Outputs

The equivalent circuit of the divider outputs is shown on the below. The outputs require a DC return path capable of handling ~35mA per side. If DC coupling is employed, the DC resistance of the receiving circuits should be ~50 ohms (or less) to VCC to prevent excessive common mode voltage from saturating the prescaler outputs. If AC coupling is used, the perfect embodiment is shown in figure 2. The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.

The output amplitude can be adjusted over a 1.5:1 range by one of the two methods The Vadj pin voltage can be set to VCC for maximum amplituded or VCC-1.3V for an amplitude ~2/3 the max swing. Voltages between these two values will produce a linear change in output swing. Alternatively, users can use a 1k potentiometer or fixed resistor tied between Vadj and VCC. Resistor values approaching 0 ohms will lead to the maximum swing, while values approaching 1k will lead to the minimum output swing. Users who only need/want the maximum swing should simply tie Vadj to VCC.

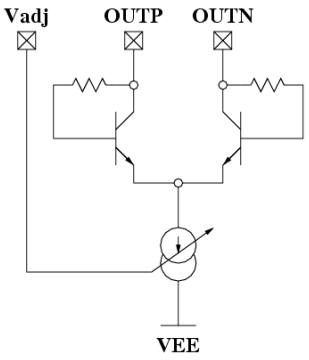


FIGURE 1:
Equivalent Circuit of Ouput Buffer

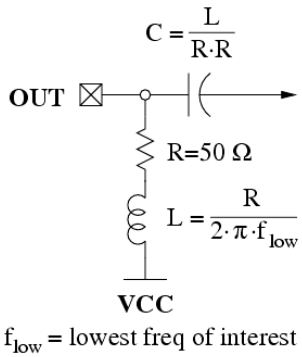


FIGURE 2:
Recommended Circuit for AC Coupled Outputs

Low Frequency Operation

Low frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to ~50MHz due to the 10dBm max input power limitation.

The values of the coupling capacitors for the high-speed inputs and outputs (I/O's) are determined by the lowest frequency the IC will be operated at.

$$C >> \frac{1}{2 \cdot \pi \cdot 50\Omega \cdot f_{lowest}}$$

For example to use the device below 30kHz, coupling capacitors should be larger than 0.1uF.

Temperature Diode

An optional on chip temperature diode is provided for users interested in evaluating the IC's temperature. A single resistor to VCC establishes a nominal current thru the diode. The voltage developed across the temperature pin (pin 8) referenced to VEE (pin 9) can then be used to indicate the surface temperature of the IC. The plot below was obtained by forcing a fixed current thru the diode for an unbiased device at multiple temperatures and fitting a line to the data to allow extrapolation over a range of temperatures.

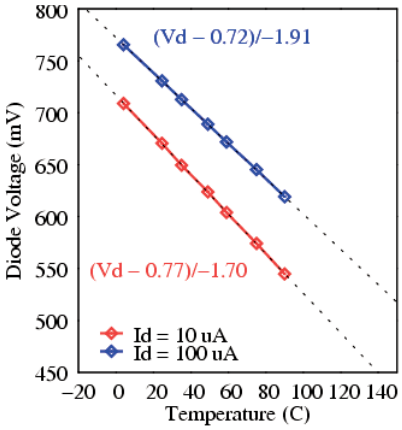


Figure 3:
Diode Voltage vs Temp for 2 Bias Currents

Package Heatsink

The package backside provides the primary heat conduction path and should be attached to a good heatsink on the PC board to maximize preformance. User PC boards should maximize the contact area to the package paddle and contain an array of vias to aid thermal conduction to either a backside heatsink or internal copper planes.

IC Assembly

The device is designed to operate with either single-ended or differential inputs. Figures 4, 5 & 6 show the IC assembly diagrams for positive and negative supply voltages. In either case the supply should be capacitively bypassed to the ground to provide a good AC ground over the frequency range of interest. The backside of the chip should be connected to a good thermal heat sink.

All RF I/O's are connected to VCC through on-chip termination resistors. This implies that when VCC is not DC grounded (as in the case of positive supply), the RF I/O's should be AC coupled through series capacitors unless the connecting circuit can generate the correct levels through level shifting.

Negative CML Logic Levels for DC Coupling (T=25 ºC)

Assuming 50Ω Terminations at Inputs and Outputs

Parameter		Minimum	Typical	Maximum
Differential	$Logic\ Input_{high}$	Vcc	Vcc	Vcc
	$Logic\ Input_{low}$	Vcc - 0.05V	Vcc - 0.3V	Vcc - 1V
Single	$Logic\ Input_{high}$	Vcc + 0.05V	Vcc + 0.3V	Vcc + 1V
	$Logic\ Input_{low}$	Vcc - 0.05V	Vcc - 0.3V	Vcc - 1V
Differential & Single	$Logic\ Output_{high}$	Vcc - 0.9V	Vcc - 0.6V	Vcc - 0.5
	$Logic\ Output_{low}$	Vcc - 1.3V	Vcc - 1.6V	Vcc - 1.7V

Differential vs Single-Ended

The UXD20P is fully differential to maximize signal-to-noise ratios for high-speed operation. High speed inputs are terminated to VCC with on-chip resistors (refer to functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to V_{max} to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

$$I\ V_{dm}/2 + V_{cm}\ I < Vcc \geq V_{max}$$

where V_{dm} is the differential input signal and V_{cm} is the common-mode voltage.

In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC value of the waveform at IC should be equal to VCC for single-ended operation. In practice, this is easily achieved with a single capacitor on the input acting as a DC block. The value of the capacitor should be large enough to pass the lowest frequencies of interest. Use the positive terminals for single-ended operation while terminating the negative terminal to VCC.

Note that a potential oscillation mechanism exists if both inputs are static and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations. Tying unused inputs directly to VCC shorts out the internal 50Ω bias resistor, imposing a DC offset sufficient to prevent oscillations. Driving the differential inputs with DC blocks, or driving the single-ended inputs without terminating unused inputs, is not recommended without taking additional steps to eliminate the potential oscillation issues.

Positive Supply (AC Coupling)

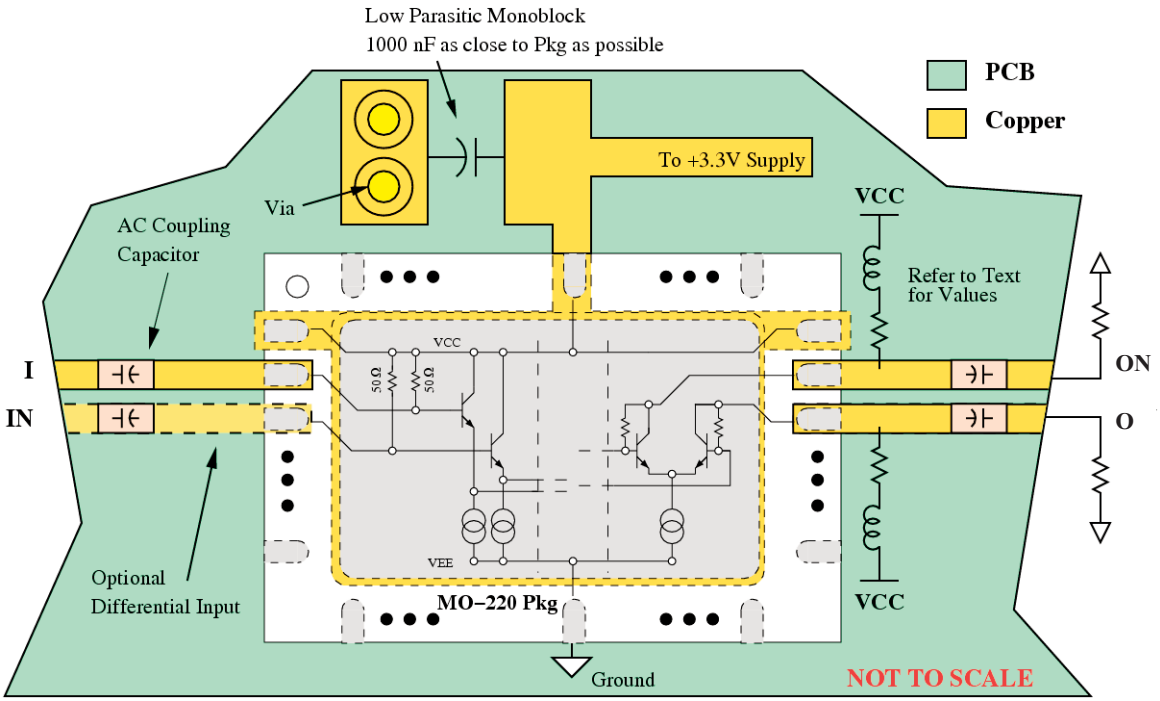


Figure 4:
Biasing recommendations for positive supply with AC coupling applications

Negative Supply (DC Coupling)

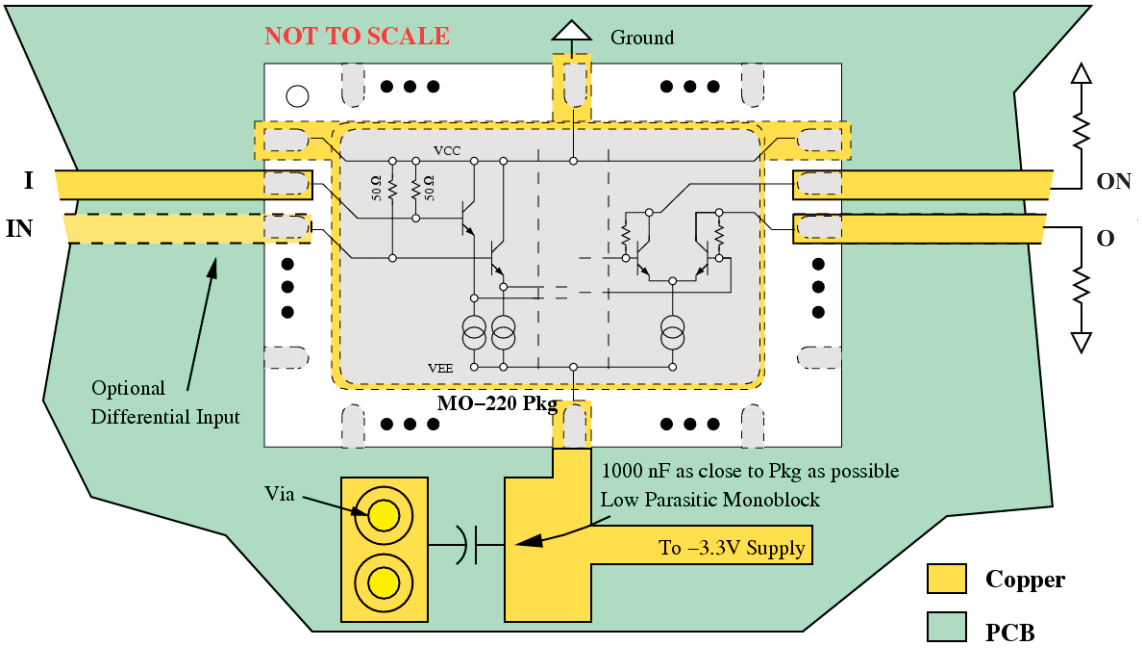


Figure 5:
Biasing recommendations for negative supply with DC coupling applications

Negative Supply (AC Coupling)

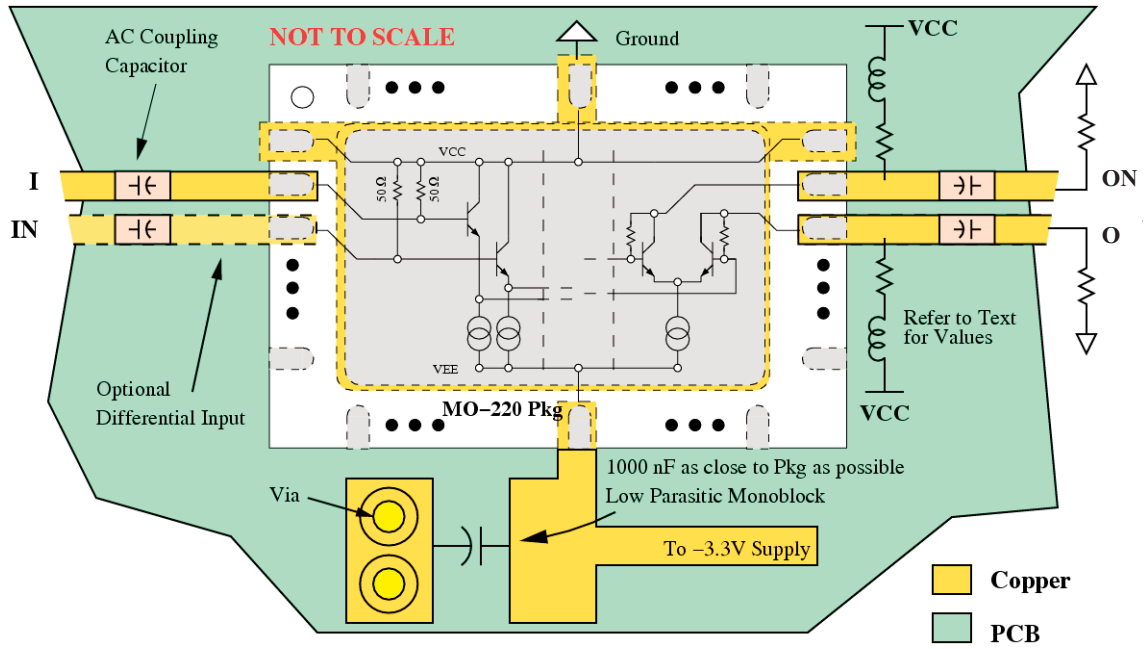
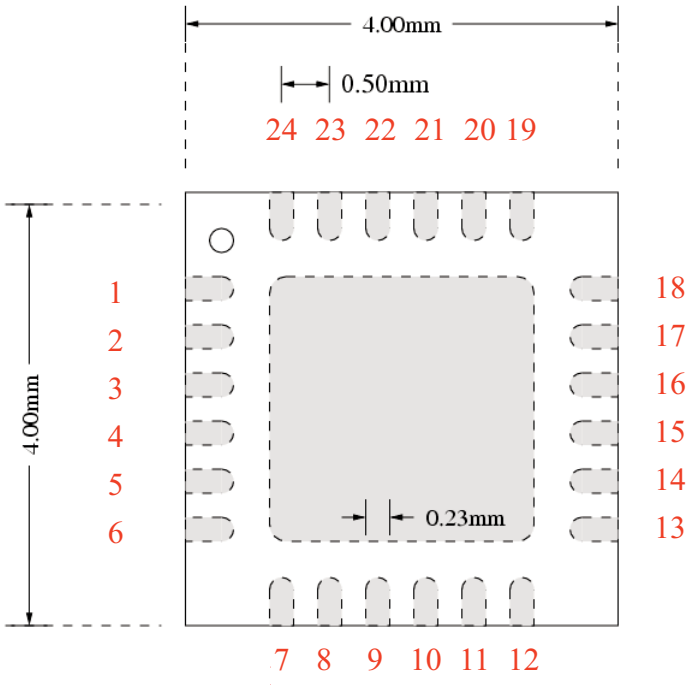


Figure 6:
Biasing recommendations for negative supply with AC coupling applications

UXD20P Physical Characteristics



Pkg Size:	**4.00 x 4.00 mm**
Pkg Size Tolerance:	**+/- 0.25 mm**
Pkg Thickness:	**0.9 +/- 0.1 mm**
Pad Dimensions:	**0.25 x 0.4 mm**
Center Paddle:	**2.2 x 2.2 mm**
JEDEC Designator:	**MO-220**

TOP VIEW

UXD20P Pin Definition

Pin Function		Operational Notes
1,3,5,6,7,13,15,17,19,20 (Vcc)	RF and DC Ground	0V (+3.3V when using positive supply)
9,23,24 (Vee)	Negative Supply Voltage	Nominally -3.3V (0V when using positive supply)
2 (INP)	Divider Input	Positive Terminal of differential input
4 (INN)	Divider Input	Negative Terminal of differential input
8 (Temp)	Temperature Diode	IC Surface temperature, Refer to text
12,11,10 (NC)	No Connect	-
14 (VADJ)	Output Amplitude Control	Tie to VCC for max swing. Refer to text
16 (OUTP)	Divider Output	Postive Terminal of differential output
18 (OUTN)	Divider Output	Negative Terminal of differential output
21 (SelB)	Divider Mode	Divider Select Line, Refer to Table 1
22 (SelA)	Divider Mode	Divider Select Line, Refer to Table 1
Paddle	Package Paddle	Tie to heatsink, Refer to text. Tie to +3.3V for positive supply and ground for negative supply.

Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage (VCC - VEE)	4.0	V
RF input power (INP, INN)	+10	dBm
Operating Temperature	-40 to 85	ºC
Storage Temperature	-85 to 125	ºC